10 GHz clock recovery using an opto-electronic phase-locked loop based on four-wave mixing in periodically-poled lithium niobate

Fausto Gómez, Cédric Ware and Didier Erasme
GET/Télécom Paris (ENST), Communications and Electronics dept.
46 rue Barrault, 75634 Paris CEDEX 13, France
fausto.gomez@enst.fr, cedric.ware@enst.fr

Raimund Ricken, Viktor Quiring and Wolfgang Sohler
Universität Paderborn, Fakultät für Naturwissenschaften
Department Physik — Angewandte Physik, Warburgerstraße 100, D-33098 Paderborn

Abstract: Successful 10 GHz clock recovery is presented, using an opto-electronic PLL based on three-wave mixing in periodically-poled lithium niobate as a phase comparator. Higher bitrates and sub-clock recovery are anticipated without modification.

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1. Introduction

Clock recovery is a critical function of any digital communications system. To replace the classical electronic phase-locked loops (PLLs) at higher bit rates, several all-optical or opto-electronic clock recovery methods are being studied; notably opto-electronic PLLs, which use the same basic scheme, replacing the up-front mixer or phase comparator by a nonlinear optical device. Systems using four-wave mixing or cross-gain modulation in semiconductor optical amplifiers have been previously demonstrated [1–3].

This paper presents—for the first time, to our knowledge—an opto-electronic PLL where three-wave mixing in a periodically-poled lithium niobate device (PPLN) provides the phase comparator operation. Since PPLN is passive, it generates no amplified spontaneous emission noise; also, the error signal is in the visible (763 nm), therefore easily separated from infrared input signals by a silicon photodetector.

2. Experimental setup

The clock recovery system is described in figure 1. The three basic blocks of a PLL can be recognized: a voltage-controlled oscillator (VCO); a phase comparator or a mixer; and a loop filter.

The VCO is a standard electronic oscillator. Its operating point is tuned by a DC voltage shifter. Its output drives the electroabsorption modulator of an integrated laser and modulator (ILM) at $\lambda_c \simeq 1550\,\text{nm}$. Thus one has an optical signal, modulated at a frequency $f_c \simeq 10\,\text{GHz}$, amplified by an erbium-doped fiber amplifier (EDFA). This forms the *clock signal*.

The clock signal is coupled into a 3-dB coupler alongside with the input signal. The latter is produced by a tunable laser set at $\lambda_s \simeq 1502\,\text{nm}$ so as to match the wavelength where the PPLN performs a sum-frequency generation: $2 \times [\lambda_c^{-1} + \lambda_s^{-1}]^{-1} = 1526\,\text{nm}$. That beam is sinusoidally modulated at $f_s \simeq 10\,\text{GHz}$ by an external modulator.

Upon injection into the PPLN, these signals generate a three-wave mixing beam at 763 nm, detected by a silicon avalanche photodetector, insensitive to the infrared input signals which would otherwise blind it. This *error signal*'s envelope depends on the input and clock signals' intercorrelation—in the same way as in an optical autocorrelator.

If the modulation frequencies f_s and f_c are not equal, the photodetector output signal bears a low-frequency component at $|f_s - f_c|$. (Other components, at the sum frequency, are filtered out by the photodetector, whose bandwidth is only a few tens of MHz.) On the other hand, if the PLL is locked in: $f_s = f_c$ (or even $f_s = N \times f_c$ for sub-clock recovery), the error signal is constant, and its level depends on the delay between the input and clock pulse trains. This behavior therefore mimics that of an electrical mixer, which can act as a phase comparator.

This comparator's output is low-pass filtered and shifted, then drives the VCO, which closes the loop.

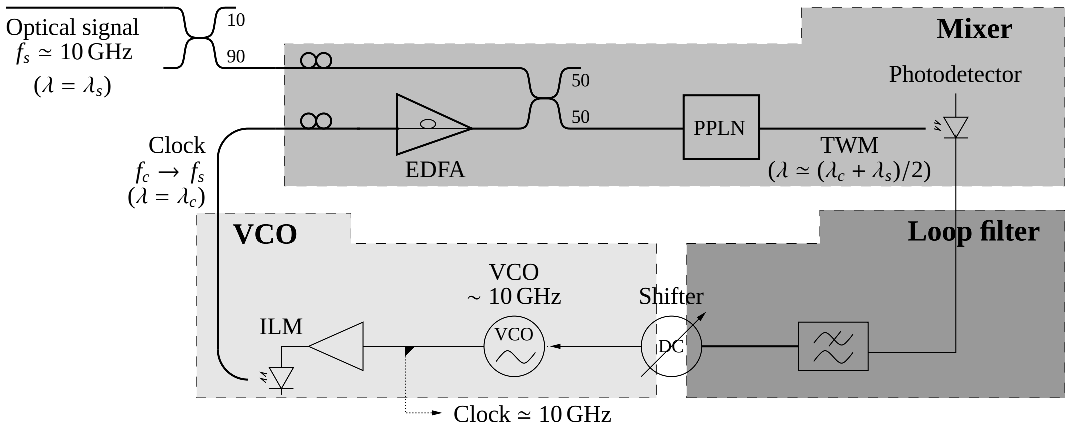
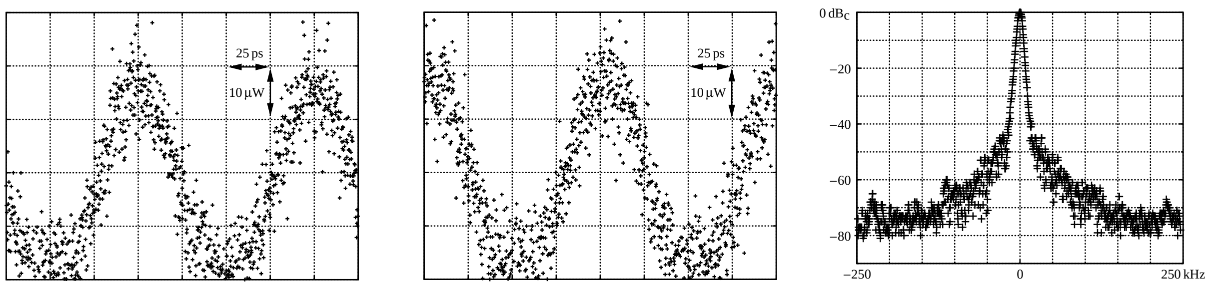


Fig. 1. Opto-electronic phase-locked loop basic scheme. Illustrates the three basic PLL blocks (VCO, mixer and filter): the “VCO” includes an integrated laser and modulator, making its output an optical pulse train; the “mixer” is based on three-wave mixing in the PPLN, detected by a silicon photodetector; the “filter” includes a voltage shifter so as to tune the VCO’s operating point.



(a) Input signal, trig. by generator (b) Input signal, trig. by recovered clock (c) Recov. clock spectrum around 10 GHz

Fig. 2. Recovered clock and signal

3. Results and discussion

Clock was successfully recovered on a 10-GHz sinusoidal optical signal. Figures 2(a) and 2(b) show a sampling oscilloscope trace of the input signal triggered respectively by the synthesizer clock and the recovered clock. The latter clock’s spectrum is shown figure 2(c). The PLL is locked in, tracking bandwidth varies between 6 and 11 kHz. Pedestal integration on figure 2(c) yields an electrical clock jitter estimated at 6.6 ps.

This preliminary result is subject to improvement. It is to be noted that our PPLN sample’s frequency doubling wavelength, 1526 nm, does not allow easy erbium-based amplification, which impairs the loop’s gain; also, stability is problematic due to the length of EDFA within the loop. The loop length could be minimized by integrating the phase comparator onto an optical circuit.

4. Conclusion

We have demonstrated an opto-electronic phase-locked loop based on three-wave mixing in periodically-poled lithium niobate. This device successfully recovers clock from a 10 GHz sinusoidal signal.

This scheme being based on ultrafast nonlinear effects, it should be able to reach still higher bit rates, on the order of several hundred Gbps. Also, as noted in section 2, the three-wave-mixing-based phase comparator operates as well if the signal frequency is a multiple of the clock frequency; therefore we anticipate this scheme to be capable of sub-clock extraction (e.g. 40-to-10 GHz), without modifications. The corresponding experiments remain to be done.

5. References

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