Heterojunction Field Effect Transistor (HFET)

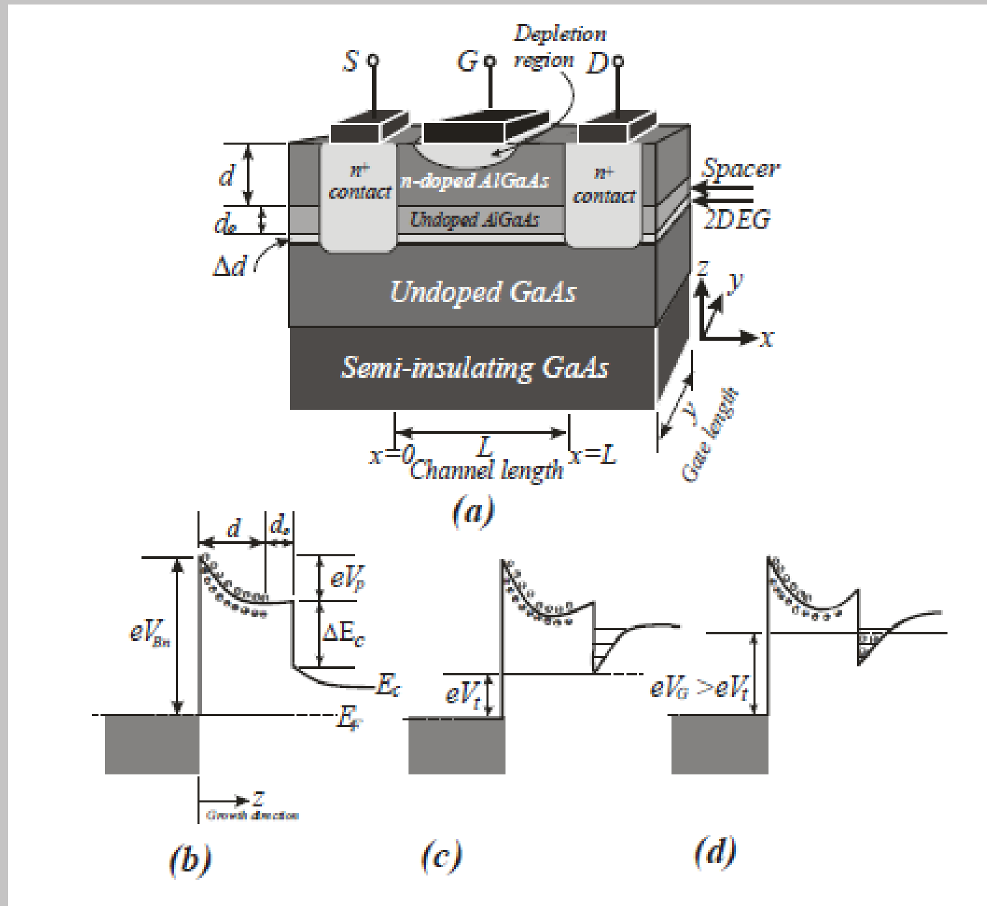


Fig. 6.13. *(a) A sketch of a MODFET based on GaAs/AlGaAs heterojunction is shown. The conduction band diagram is shown for (a) $V_G=0$, thermal equilibrium; (b) $V_G=V_T$, where V_T is the threshold voltage; and (c) $V_G>V_T$.*

Heterojunction Field Effect Transistor (HFET)

The pinch-off voltage can be obtained by integrating the electric field over the total thickness of the doped AlGaAs barrier. Assuming that the dopant density, N_d, is uniform across the barrier, V_p can be written as

$$V_p = \frac{e}{\epsilon_s} \int_0^d N_d z \mathrm{d}z = \frac{e N_d d^2}{2\epsilon_s}$$

The threshold voltage can be written as

$$eV_t = eV_{Bn} - \Delta E_c - eV_p,$$

where eV_{Bn} is the Schottky barrier height.

When V_t is positive, the MODFET is normally off. This is called the enhancement mode. On the other hand, the normally on MODFET corresponds to the depletion mode or negative V_t.

Heterojunction Field Effect Transistor (HFET)

a charge sheet or 2DEG density, $\mathcal{N}_s$, is induced by the gate at the heterojunction interface, which can be given as

$$\mathcal{N}_s = \frac{C_i(V_G - V_t - V_x)}{e}$$

where the capacitance per unit area, C_i, is given as

$$C_i = \frac{\epsilon_s}{d + d_0 + \Delta d}$$

where Δd is the thickness of the channel or the width of the triangular quantum well. The potential V_x is the channel potential with respect to the ground (source). Thus, V_x varies through the channel from zero at the source terminal to V_D at the drain terminal. the 2DEG density increases as the positive gate voltage, V_G, (forward bias) increases. For negative V_G, $\mathcal{N}_s$ is reduced drastically and the device is turned off.

Heterojunction Field Effect Transistor (HFET)

drain current, I_D, at any point along the channel of the MODFET

$$I_D = y e \mu_n N_s \mathcal{E}_x$$

where $\mathcal{E}_x$ is the electric field at any point along the channel.

$$I_D = y \mu_n \epsilon_s \frac{(V_G - V_t - V_x)}{(d + d_0 + \Delta d)} \frac{dV_x}{dx}$$

Integrating from source ($x = 0$ and $V_x = 0$) to the drain ($x = L$ and $V_x = V_D$) yields

$$I_D = \frac{y}{2L} \frac{\mu_n \epsilon_s}{(d + d_0 + \Delta d)} [2(V_G - V_t)V_D - V_D^2]$$

For the linear region or nonsaturation region $V_D \ll V_G - V_t$,

$$I_D = \frac{y}{L} \frac{\mu_n \epsilon_s}{(d + d_0 + \Delta d)} (V_G - V_t) V_D$$

For a large drain voltage, the depletion region reaches the channel and causes the pinch-off, where the density of the 2DEG is reduced to zero at $x = L$.

Heterojunction Field Effect Transistor (HFET)

V_D^{sat} can be obtained from

$$V_D^{sat} = V_G - V_t$$

The saturation current can now be obtained by replacing V_D with V_D^{sat}

$$I_D^{sat} = \frac{y}{2L} \frac{\mu_n \epsilon_s}{(d + d_0 + \Delta d)} (V_G - V_t)^2$$

The transconductance is obtained by

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D = \text{constant}}$$

which yields

$$g_m = \frac{y}{L} \frac{\mu_n \epsilon_s}{(d + d_0 + \Delta d)} (V_G - V_t)$$

The electric field along the channel reaches high values in high speed devices, causing carrier velocity saturation.

The drain current in the high speed operation mode can be written as

$$I_D^{hs} = y e \mu_n \mathcal{N}_s \epsilon_x = y e v_s \mathcal{N}_s = y v_s C_i (V_G - V_t)$$

Heterojunction Field Effect Transistor (HFET)

Using the definition of the cut-off frequency

$$2\pi f_{\mathrm{T}} C_{\mathrm{G}} v_{\mathrm{g}} = g_{\mathrm{m}} v_{\mathrm{g}} \Rightarrow f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{G}}}$$

knowing that the capacitance C_{i} defined

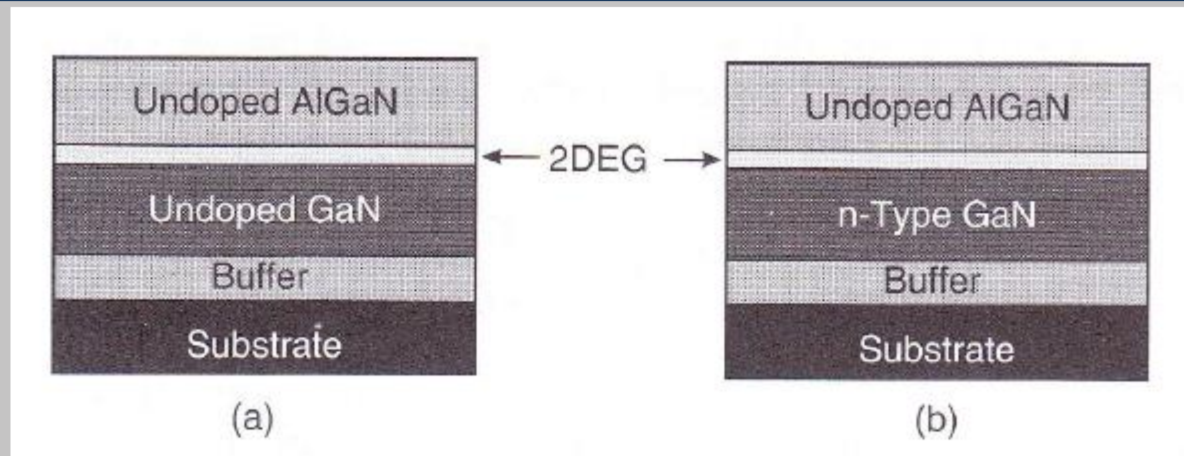
$$C_{\mathrm{i}} = \frac{\epsilon_s}{d + d_0 + \Delta d}$$

one can express the cut-off frequency as

$$f_{\mathrm{T}} = \frac{v_{\mathrm{s}}}{2\pi \left(L + \frac{C_{\mathrm{p}}}{y C_{\mathrm{i}}} \right)}$$

where C_{p} is the total parasitic capacitance.

GaN/AlGaN Heterojunction Field Effect Transitor (HFET)



Two sketches of the most common GaN/AlGaN HFET structures.

A simple electrostatic analysis shows that the sheet carrier concentration, $\mathcal{N}_s$, of the 2DEG at the GaN/$Al_xGa_{1-x}N$ heterojunction interface should be given approximately by (Morkoç and Yu)

$$\mathcal{N}_s = \sigma_{pol}/e - (\epsilon_{AlGaN}/de^2)(e\phi_b + E_F - \Delta E_c) + \tfrac{1}{2}N_d d$$

The polarization-induced sheet charge density σ_{pol} at the GaN/$Al_xGa_{1-x}N$ heterojunction interface is

$$\sigma_{pol}/e \approx -2[e_{31} - (c_{13}/c_{33})e_{33}](a_{GaN}/a_{AlN} - 1)x + P_{sp,z}^{GaN} - P_{sp,z}^{AlGaN}$$

$\sigma_{pol} \approx (5\text{–}6.5) \times 10^{13} x e/\text{cm}^2$ where x is the Al mole fraction

Heterojunction Field Effect Transitor (HFET)

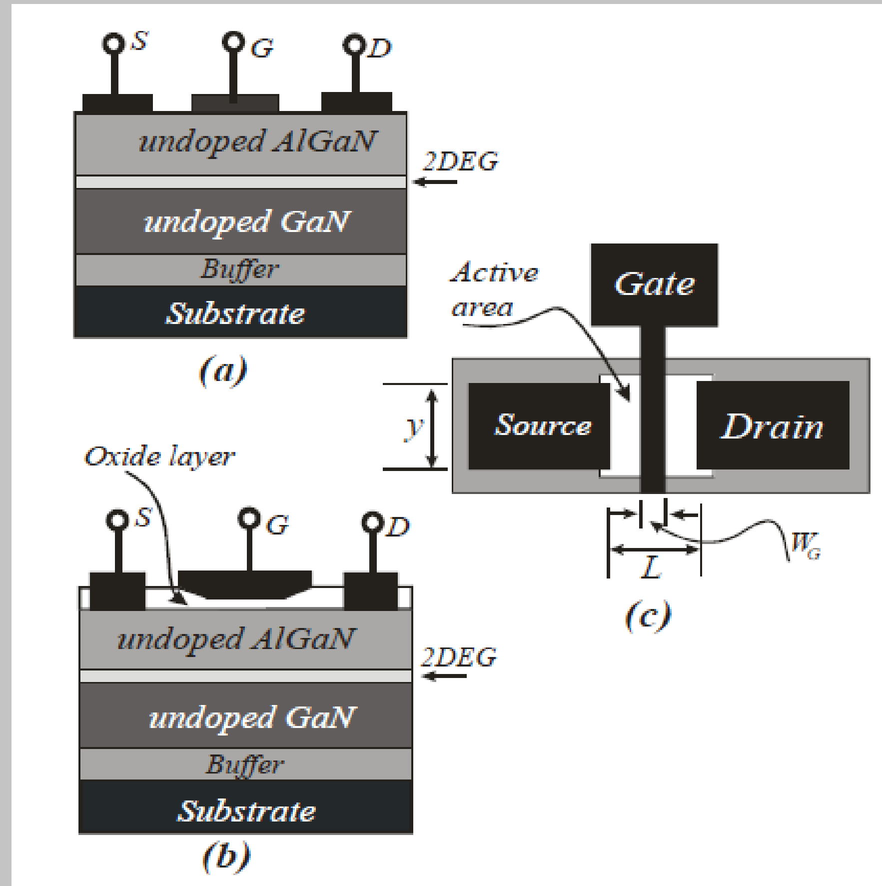


Fig. 6.15. *(a) A schematic structure of a GaN/AlGaN HFET showing the gate, drain, and source meals deposited directly on the surface of the AlGaN layer. (b) A schematic structure of GaN/AlGaN HEFT with an additional oxide layer deposited underneath the gate metal. (c) A sketch of a top view of an HFET.*

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GaN/AlGaN Heterojunction Field Effect Transitor (HFET)

The drain current–voltage ($I_D - V_D$) characteristics of the GaN/AlGaN HFET

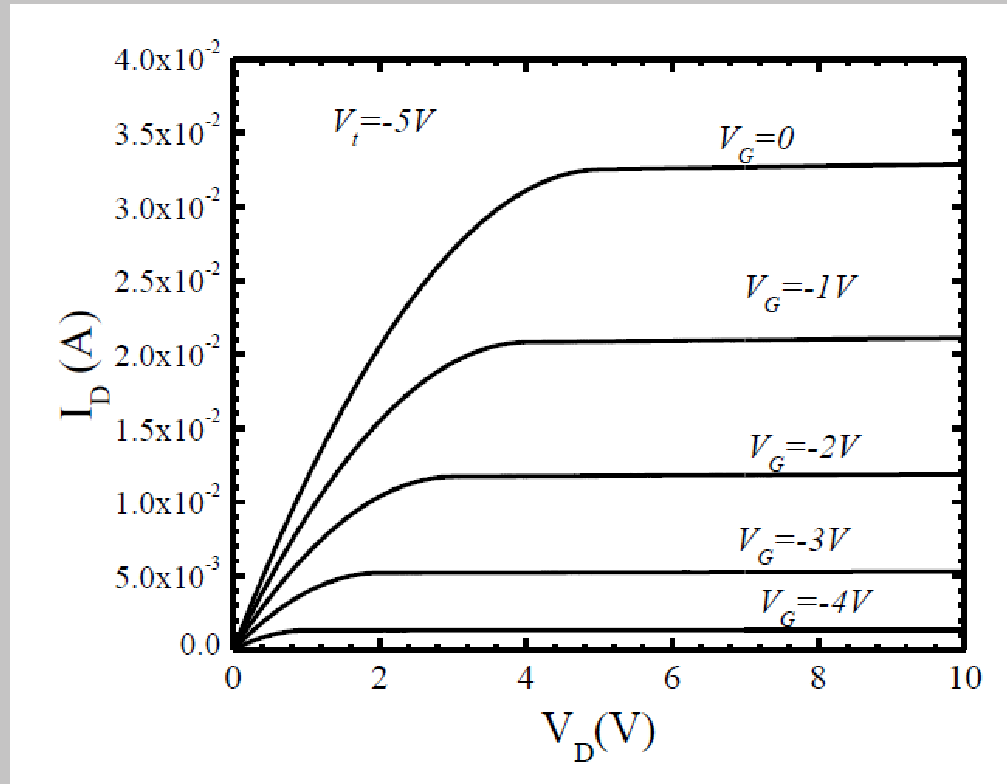

Fig. 6.16. I_D-V_D characteristic curves of a GaN/AlGaN single channel HFET with a threshold voltage of -5V, channel length of 0.5 μm, and gate length of 20 μm.

g_m versus V_{DS} eines AlGaN/GaN HEMTs

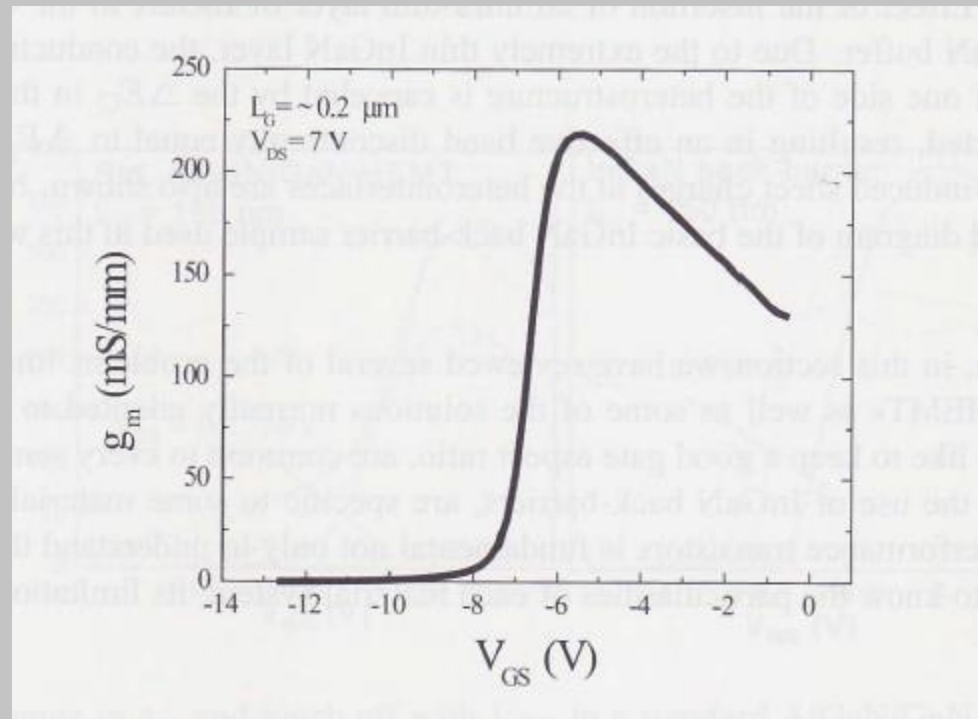

Figure 8.38: Decrease of g_m as the drain current increases (i.e. V_{GS} increases) in an AlGaN/GaN HEMT.

Heterojunction Field Effect Transitor (HFET)

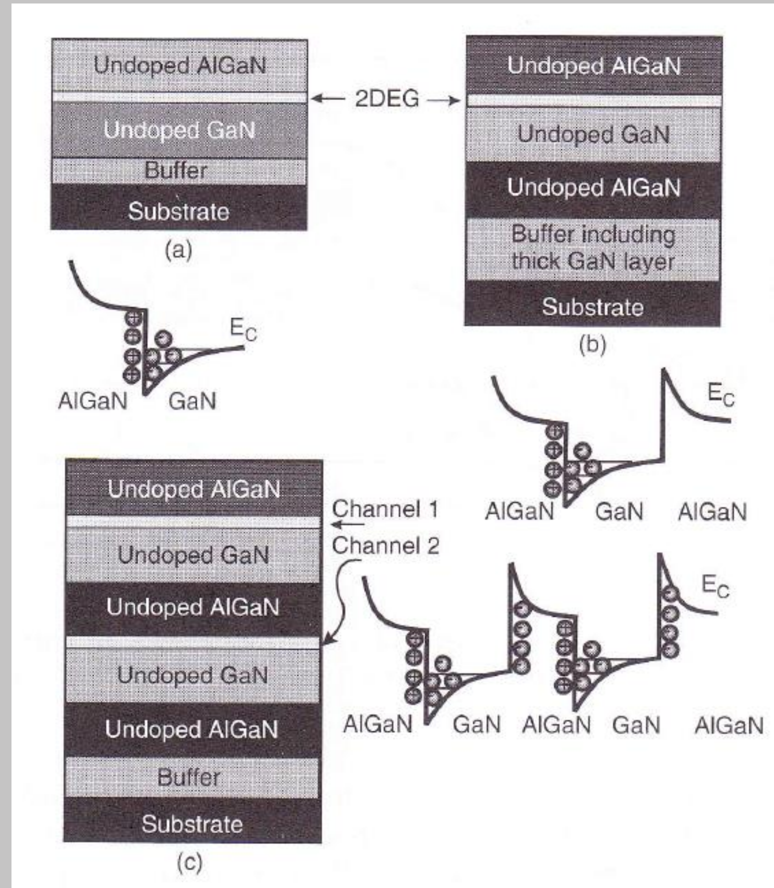

FIGURE 6.17 (a) A basic single heterojunction structure of a GaN/AlGaN HFET. (b) A double heterojunction structure. (c) Two channel structures. The conduction energy band diagram is sketched for the three structures showing the spontaneous polarization-induced charge distribution.

MESFET mit und ohne Drain-Source Spannung

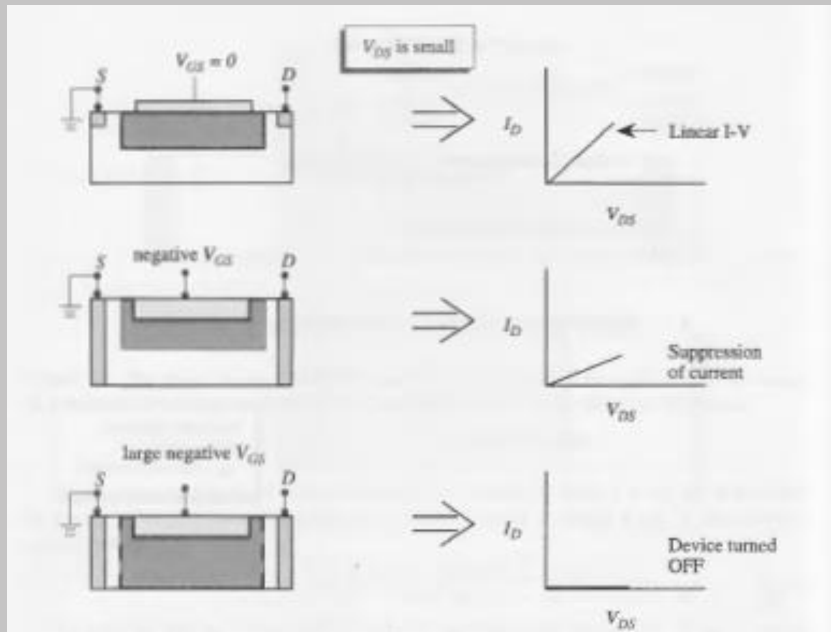

Figure 8.4: (a) Depletion width and channel in a JFET or MESFET under zero gate bias. The channel has a large opening. Such a device is called a depletion-mode device; (b) the device with a negative gate bias showing reduction in the channel opening and current; (c) the gate bias is large and negative and the channel is pinched off with current in the channel zero.

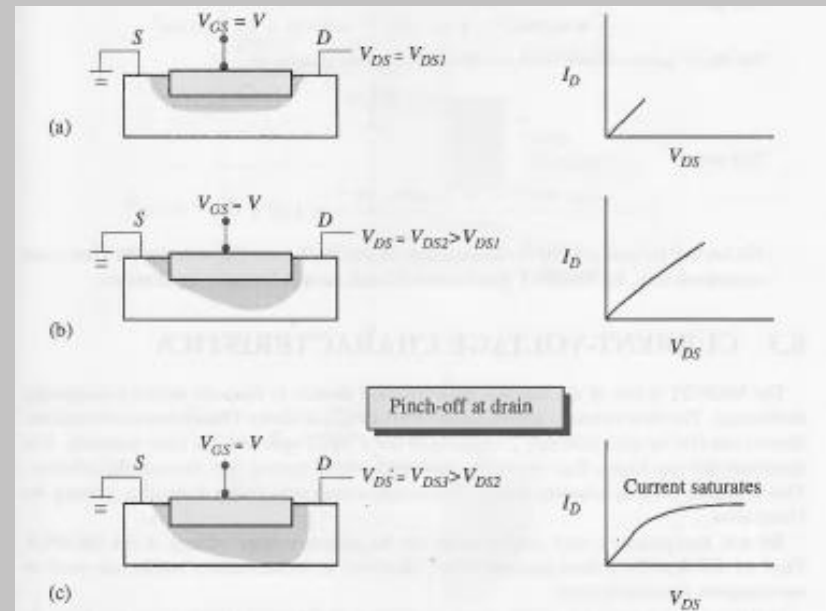

Figure 8.5: The effect of increased drain bias at a fixed gate bias. (a) the drain bias is small; (b) the drain bias is increased and the channel is constricted near the drain; (c) the drain bias is increased to the point that the channel is pinched off at the drain side. The drain current saturates as shown.